Amendments to the Claims

1-2. (Cancelled)

3. (Previously Presented) A circuit comprising:

an input port having an input signal voltage;

an output port having an output voltage; and

a field-effect-transistor (FET) having a gate, a first terminal, and a second terminal;

wherein the gate and the first terminal are each connected to the input port, and the second terminal is connected to the output port;

wherein the FET has a device width, wherein the FET has a leakage current in excess of 1 micro ampere per micron of device width; and

wherein the output voltage is indicative of a local time-average maximum of the input signal voltage.

4. (Previously Presented) A method to provide an output voltage indicative of a local time-average maximum of an input signal voltage, the method comprising:

operating a field-effect transistor (FET) in its sub-threshold region when in steady state and the input signal voltage is stationary, the FET having a gate, a first terminal, and a second terminal, wherein the FET has a leakage current in excess of 1 micro ampere per micron of device width, wherein the gate and the first terminal are each connected to an input port, and the second terminal is connected to an output port;

providing the input signal voltage to the input port; and

sampling the output voltage at the output port to provide a local time-average maximum of the input signal voltage.

5. (Cancelled)

6. (Previously Presented) A circuit to provide direct current (DC) offset correction to an input signal voltage, the circuit comprising:

an input port having the input signal voltage;

a field-effect-transistor (FET) having a gate, a first terminal, and a second terminal, wherein the gate and the first terminal are each connected to the input port, wherein the second terminal has a DC offset correction voltage, wherein the FET has a leakage current in excess of 1 micro ampere per micron of device width to provide the DC offset correction voltage as a local time-average maximum of the input signal voltage; and

a DC offset correction unit responsive to the DC offset correction voltage to subtract the DC offset correction voltage from the input signal voltage.

7-8. (Cancelled)

9. (Previously Presented) A circuit comprising:

an input port having an input signal voltage;

an output port having an output voltage; and

a field-effect-transistor (FET) having a gate, a first terminal, and a second terminal;

wherein the first terminal is connected to the input port, and the gate and the second terminal are each connected to the output port;

wherein the FET has a device width, wherein the FET has a leakage current in excess of 1 micro ampere per micron of device width; and

wherein the output voltage is a local time-average minimum of the input signal voltage.

10. (Previously Presented) A method to provide an output voltage indicative of a local time-average minimum of an input signal voltage, the method comprising:

operating a field-effect transistor (FET) in its sub-threshold region when in steady state and the input signal voltage is stationary, the FET having a gate, a first terminal, and a second terminal, wherein the FET has a leakage current in excess of 1 micro ampere per micron of device width, wherein the first terminal is connected to an input port, and the gate and the second terminal are each connected to an output port;

providing the input signal voltage to the input port; and

sampling the output voltage at the output port to provide a local time-average minimum of the input signal voltage.

11. (Cancelled)

12. (Previously Presented) A circuit to provide direct current (DC) offset correction to an input signal voltage, the circuit comprising:

an input port having the input signal voltage;

a field-effect-transistor (FET) having a gate, a first terminal, and a second terminal, wherein the first terminal is connected to the input port, wherein the gate and the second terminal are connected to each other and have a DC offset correction voltage; wherein the FET has a leakage current in excess of 1 micro ampere per micron of device width to provide the DC offset correction voltage as a local time-average minimum of the input signal voltage; and

a DC offset correction unit responsive to the DC offset correction voltage to subtract the DC offset correction voltage from the input signal voltage.

13-21. (Withdrawn)

22. (Currently Amended) The circuit as set forth in claim 3, further comprising an output circuit connected to the output port to provide a capacitive load ~~wherein the output voltage is indicative of a local time-average maximum of the input signal voltage~~.

23. (Currently Amended) The circuit as set forth in claim 9, further comprising an output circuit connected to the output port to provide a capacitive load ~~wherein the output voltage is indicative of a local time-average minimum of the input signal voltage~~.